This work was performed at Los Alamos National Laboratory, which is operated by the University of California for the United States Department of Energy under contract W-7405-ENG-36.

User's Guide to the Multiple-Independent Detector System

Los Alamos National Laboratory
Los Alamos, New Mexico 87545

This work was supported by the US Department of Energy, Office of Basic Energy Sciences.

Edited by Sharon Crane

LA-9764-M
Manual

UC-37
Issued: July 1983

User's Guide to the Multiple-Independent Detector System

P. A. Seeger

Los Alamos National Laboratory
Los Alamos, New Mexico 87545

USER'S GUIDE TO THE MULTIPLE-INDEPENDENT DETECTOR SYSTEM

by

P. A. Seeger

ABSTRACT

The multiplexing scheme used at the Weapons Neutron Research Facility for arrays of individual detectors is presented. Information is given to allow a user to configure an instrument, to connect and test modules, to monitor operation, and to diagnose faults.

I. INTRODUCTION

The first detector systems used for diffraction studies at the Weapons Neutron Research (WNR) Facility were "time-focused" arrays of ^{3}He proportional counters. That is, the individual detectors were arranged geometrically on loci of constant L sin θ so that elastically scattered neutrons corresponding to any particular lattice spacing would reach all detectors at the same time. Many detectors then could be ganged together, minimizing the electronics and the computer memory space needed.

Much greater versatility in detector geometry is possible if the detectors are not ganged, but instead have individual electronic pathways and separate data areas in computer memory. This also allows higher data rates. This manual describes the philosophy, implementation, and use of the Multiple-Independent Detector System (MIDS) installed now on several instruments at WNR.

II. DESIGN GOALS

Although commercial preamplifiers, amplifiers, and discriminators have advantages in versatility, reliability, and familiarity, their disadvantages in cost, power consumption, rack space, and number of adjustments make their use impractical for arrays with several dozens of detectors. A prime goal in the development of MIDS was to reduce the cost of electronics, from about $1 200 per channel to approximately $200 per channel. To do this, we give up the versatility of adjustable gains, pulse time constants, and individual lower and upper discriminator levels. Gain is fixed during construction by component selection. Modules are standardized so far as practical, and the

user can only make global adjustments in gas multiplication and lower-level discriminator setting.

A second design goal was to minimize dead time per event, to allow for anticipated high instantaneous count rates when the proton storage ring is operational. Total encoding time has been reduced to about 400 ns, but this is at the expense of high sensitivity to noise (compared to commercial pulse shaping with 2 μs-time constants and about 5 μs of dead time). Note that this noise sensitivity mandates careful studying of the grounding for each instrument (i.e., signal return paths, electrostatic shielding, and power-supply earthing) and maintaining the integrity of the grounds after the optimum configuration is established.

The third design goal was to simplify the individual circuit modules, as an aid to construction, maintenance, and operation of the system. Using hybrid and integrated circuits rather than discrete components does simplify the individual modules and also helps keep the modules small.

III. SYSTEM OVERVIEW

Figure 1 is a simplified block diagram of a MIDS. The Shaping Preamplifiers (79Y-197934) are housed in the same enclosure as the detectors, receiving power from the 32-Channel Proportional-Counter Multiplexer (79Y-197902), which is a NIM module (note that ±6-V power supplies and forced-air cooling are required for this module in the NIM bin). Generally, the detector high voltage is also supplied from a (commercial) NIM module. The outputs of the multiplexer are a 5-bit binary number and a time-strobe signal.

The customary experimental arrangement at WNR includes low-level analog circuitry close to the detector (downstairs) and high-level or digital signals sent through several hundred meters of 50-Ω cable to the data acquisition computer (upstairs). A separate line-driver module is required; this may be incorporated in a second-level multiplexer if more than 32 detectors are used. Three versions exist: a simple Latching Line Driver (79Y-197953), a Two-Way or 64-Channel Multiplexer (79Y-197955), and a Four-Way or 128-Channel Multiplexer (79Y-197954). At the receiving end, a latching buffer module containing optoisolators (79Y-197952) is used to avoid injecting noise into the system through the upstairs/downstairs ground loop. Such precautions are necessary at WNR because the "clean" ground isn't clean. For instance, when using an oscilloscope to look at the unbuffered signals, it may help to use it in the differential mode if noise is a problem.

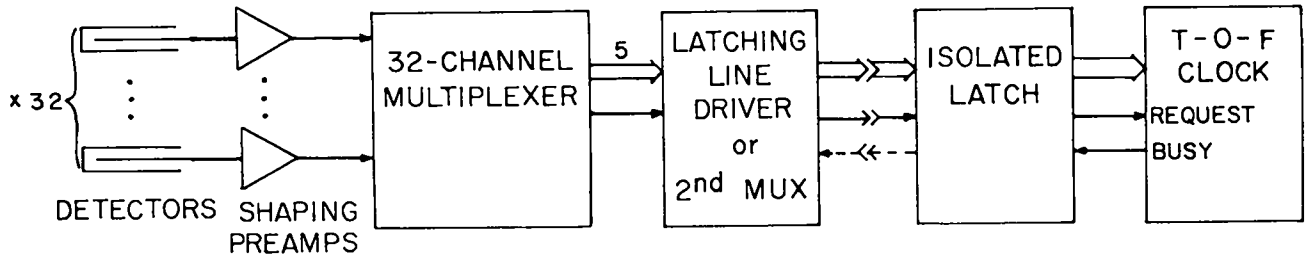


Fig. 1.
Simplified Multiple-Independent Detector System. Additional detectors and 32-channel multiplexers may be combined in an appropriate second-level multiplexer. The break indicates long cable runs.

Outputs of the buffer are compatible with the Fast Digital Data-Acquisition System (FDDAS) (Ref. 1). The next module in most applications is a Model 6 Time-of-Flight Clock (79Y-197938), which forms an event descriptor of up to 24 bits by concatenating the detector identification bits with time information. The clock is a CAMAC module, with output either through the CAMAC dataway or on a front-panel FDDAS connector. Handshaking signals provide for connecting through FDDAS to modules for further processing or to an auto-incrementing memory.[1] The handshake must propagate back to the isolator/latch to inform it that the datum was received so that it may latch the next event. Provision is also made for handshaking back to the line driver. This last link is not recommended generally for two reasons: first, the round-trip signal propagation time of about 1 μs may increase dead time unnecessarily; and second, the presence of an "upstairs" ground in the "downstairs" environment increases probability of an accidental ground loop.

IV. SHAPING PREAMPLIFIER, 79Y-197934

The electrical and mechanical characteristics of the preamplifiers must be considered in instrument design, but normally the user would not need to deal with them. The circuit diagram is given in Fig. 2; the printed circuit and the parts layout are shown in Fig. 3.

A. Detector Connection

There are pads on the preamp card for high-voltage filtering and for the anode and last-dynode resistors for a photomultiplier tube. However, if high voltage exceeds 1 kV, we do not recommend using these component locations nor do we recommend having such a high voltage anywhere on the surface of the card, because of noise generated by leakage. Stand-offs may be installed on the card, or the high voltage may be distributed on a buss (of reasonably large diameter) with individual current-limiting resistors to each detector.

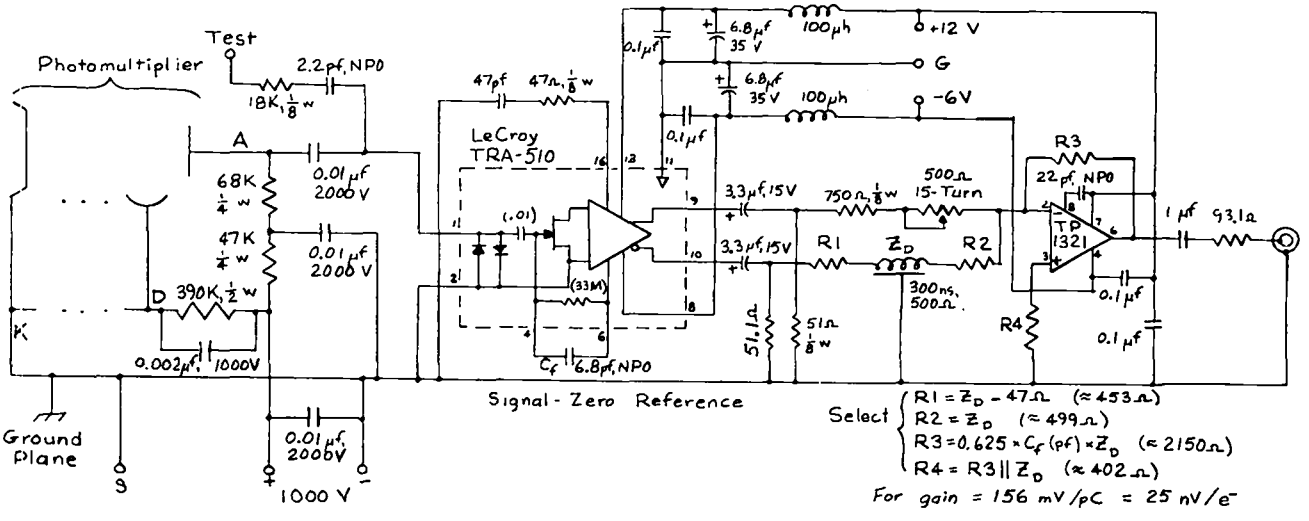


Fig. 2
Shaping Preamp (79Y-197934). High-voltage filtering components are generally omitted, and the signal is brought through an external voltage-isolation capacitor to pin 1 of the TRA-510.

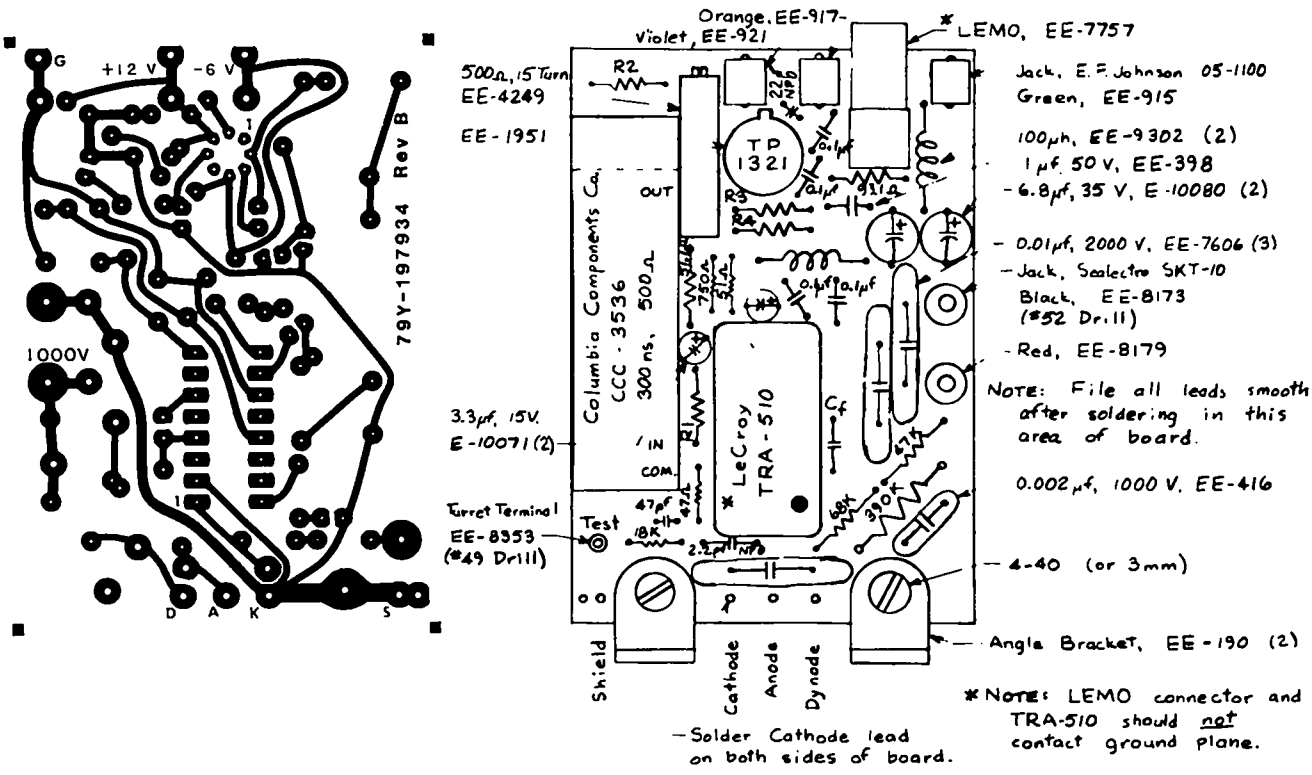


Fig. 3
Printed circuit and parts layout of shaping preamp. Components in the lower right are generally omitted, and mounting hardware varies. The delay line, C_f, R1, R2, R3, and R4 are individually selected.

For photomultipliers, three pads at the input edge of the card are labeled D (dynode), A (anode), and K (cathode). The cathode lead must be soldered on both sides of the card.

For gas detectors, the high-voltage isolation capacitor may be removed from the card and attached directly to the detector. Input is then connected to the pad between K and pin 1 of the integrated circuit. This lead must have the minimum possible capacitance to ground: it must be short and of very fine wire, and it must not be twisted with or too close to a ground wire. There must be a ground wire from K (solder on both sides of the card) to a point as close as possible to the individual detector shell.

The high-voltage isolation capacitor must be large compared to detector capacitance, but for protection of the preamp input against arcing in the detector, the capacitor must be less than 2 $\mu F/V_{max}$, where V_{max} is the highest voltage ever to be encountered. A value of 500 pF is generally a good compromise ("safe" to 4 kV, with a signal loss of 2 percent).

B. Power and Ground(s)

The card requires power supplies of +12 V (orange terminal), 0 V (green terminal), and -6 V (violet terminal). As shown in Fig. 4, we generally use pins 18-20 of a 20-pin coaxicon connector block. Typical current requirements are 15 mA of +12 V and 3 mA of -6 V per preamp. Note that the 0-V wire, which carries 12 mA per preamp, is not connected to ground on the card, but it is assumed to be grounded at the power supply (the preamps will not work if it is

not). Additional filtering of all three lines (for instance, 6.8 μH on each) should be provided inside the preamp enclosure, as illustrated in Fig. 4.

Because we are dealing with very low level analog signals in an electrically noisy environment, perhaps with the same power supply as our high-current digital signals, we must use every practical method of shielding.[2] Generally, the cathodes (outer shells) of all detectors are common electrically, and we define some point on the framework to which they are mounted as the signal-zero reference or system "ground" point, as shown in Fig. 4. The detector enclosure should be strapped to this single point, and the high-voltage return (cable braid) should be attached here. The whole detector enclosure must be isolated from earth.

If space permits, electrostatic shields between the preamps of an array are useful, but we have made successful arrays without them.

C. Selection of Components

By using a capacitor (C_f) as its feedback element, a charge-sensitive amplifier converts an input charge to an output voltage by the relation $V = q/C_f$. Choosing C_f = 6.8 pF (+0.8 pF of stray capacitance) and voltage gain = 1.2 in the second stage, the circuit gain is 156 mV/pC or 25 nV/e^-. When the detector high voltage is set so that each neutron gives 4 x 10^5 e^-, the output pulse is -10 mV. This is well within the

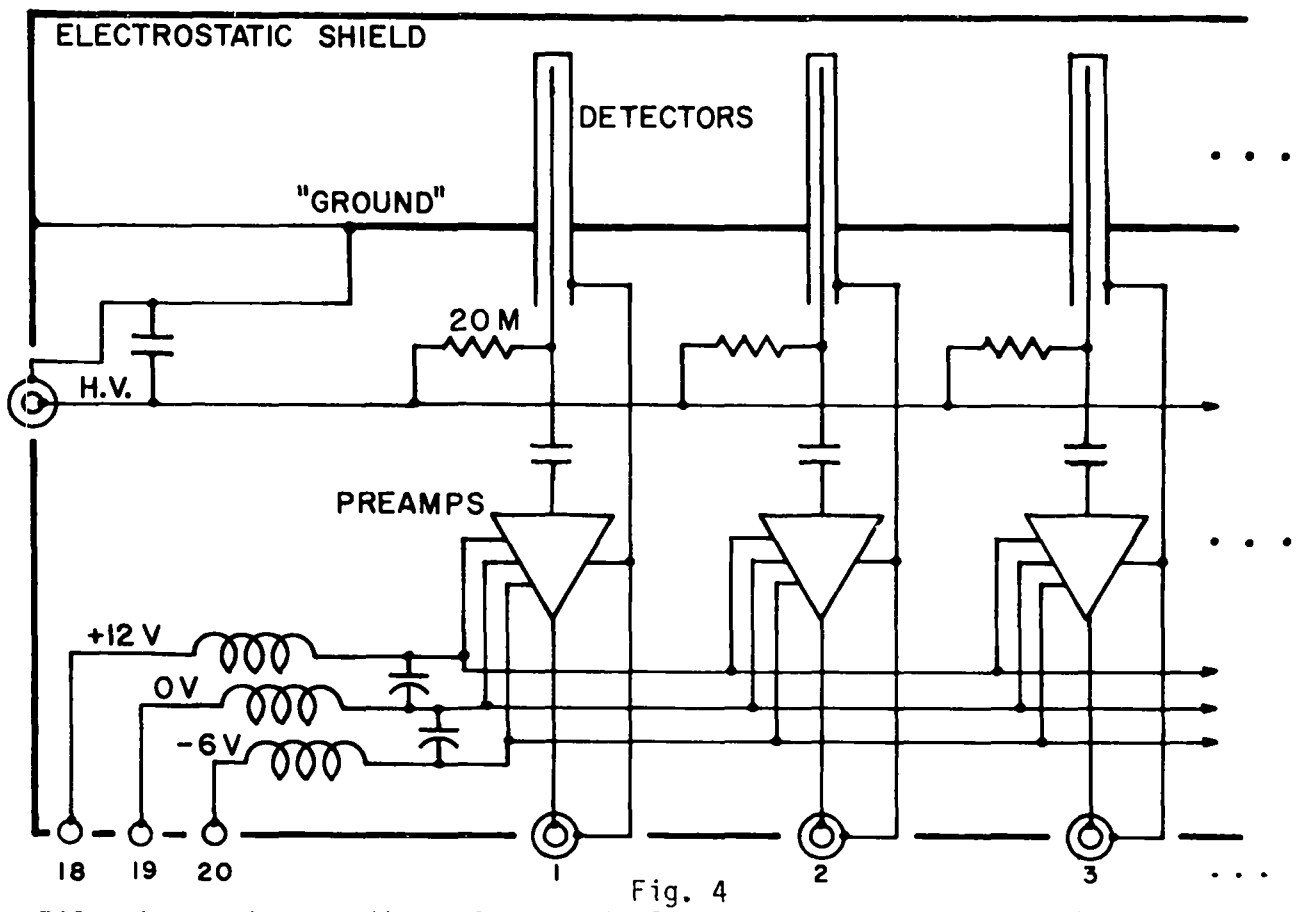


Fig. 4
Filtering and grounding of a typical detector bank. Note the attempt to separate electrically the functions of electrostatic shielding, power supply returns, signal-zero reference, and output signal returns.

specifications of the 1/2-in. diam ^{3}He proportional counters. For the 1/4-in. detectors, on the other hand, pulse size is only 3 x 10^4 e^-, so we decrease the feedback capacitance to 2.2 pF (nominal) and increase the second stage gain to 2, to obtain an output pulse of -3 mV.

The impedance Z_D of each delay line (nominally 500 Ω) must be measured for optimum termination (i.e., for minimum reflection). The delayed uninverted output of the charge-sensitive stage is added to the prompt inverted output at the input of the second stage. Second-stage gain is $R_3/2\ Z_D$, divided by 2 for impedance matching into a 93-Ω output cable.

Having measured Z_D and C_f, select resistors R_1-R_4 to obtain the required gain G (V/pC).

$$R_1 = Z_D - 47\Omega \sim 453\Omega$$

$$R_2 = Z_D \sim 499\Omega$$

$$R_3 = 4\ (C_f + 0.8\ pF)\ Z_D\ G \sim 2370\Omega$$

$$R_4 = R_3 \parallel Z_D \sim 402\Omega$$

D. Adjustment and Testing

A potentiometer on the card adjusts the gain of the undelayed signal, to balance it against the delayed signal for optimum baseline restoration. A 30-mV negative step applied to the test input may be used to represent a neutron (2.2 mV for a 1/4-in. detector).

Although intended as a baseline restoration control, this pot may also be used to trim the gains of a detector array. After adjusting all preamps for baseline, measure the pulse heights of actual neutrons in each detector and determine the average. Then adjust each gain to equalize the pulse height with the average. This should not greatly affect the baselines; if any signal is greatly different from the average, something is wrong.

Both cold-solder joints and solder bridges have been common problems on these cards. In case of difficulty, check that 0 V is grounded somewhere in the system, and that power is available on the actual op-amp pins: +12 V at pin 13 of the TRA-510 (DIP) and pin 7 of the TP1321 (can), and -6 V at pin 8 of the DIP and pin 4 of the can. Look for both output signals from the TRA-510 after the two 3.3-μF capacitors. If both are present but there is still no output, check around the TP1321. If one or both signals are missing, check continuity and check that both are terminated in 51Ω. If these corrections do not solve the problem, the TRA-510 should be replaced.

V. 32-CHANNEL PROPORTIONAL-COUNTER MULTIPLEXER, 79Y-197902

This unit is housed in a triple-wide NIM module, which requires both positive and negative 6-V supplies, and forced-air cooling. The circuit diagram is given in Fig. 5. Power requirements (including 32 preamps) are 0.5 A of +12 V, 1.5 A of +6 V, and 0.6 A of -6 V. Four units may be contained in one bin, but note that this uses all of the +12-V current available in a standard bin.

A. Theory of Operation

The multiplexer is designed around a hybrid circuit from LeCroy Research, the model PC700-150 dual amplifier/discriminator/delay/latch. Each amplifier

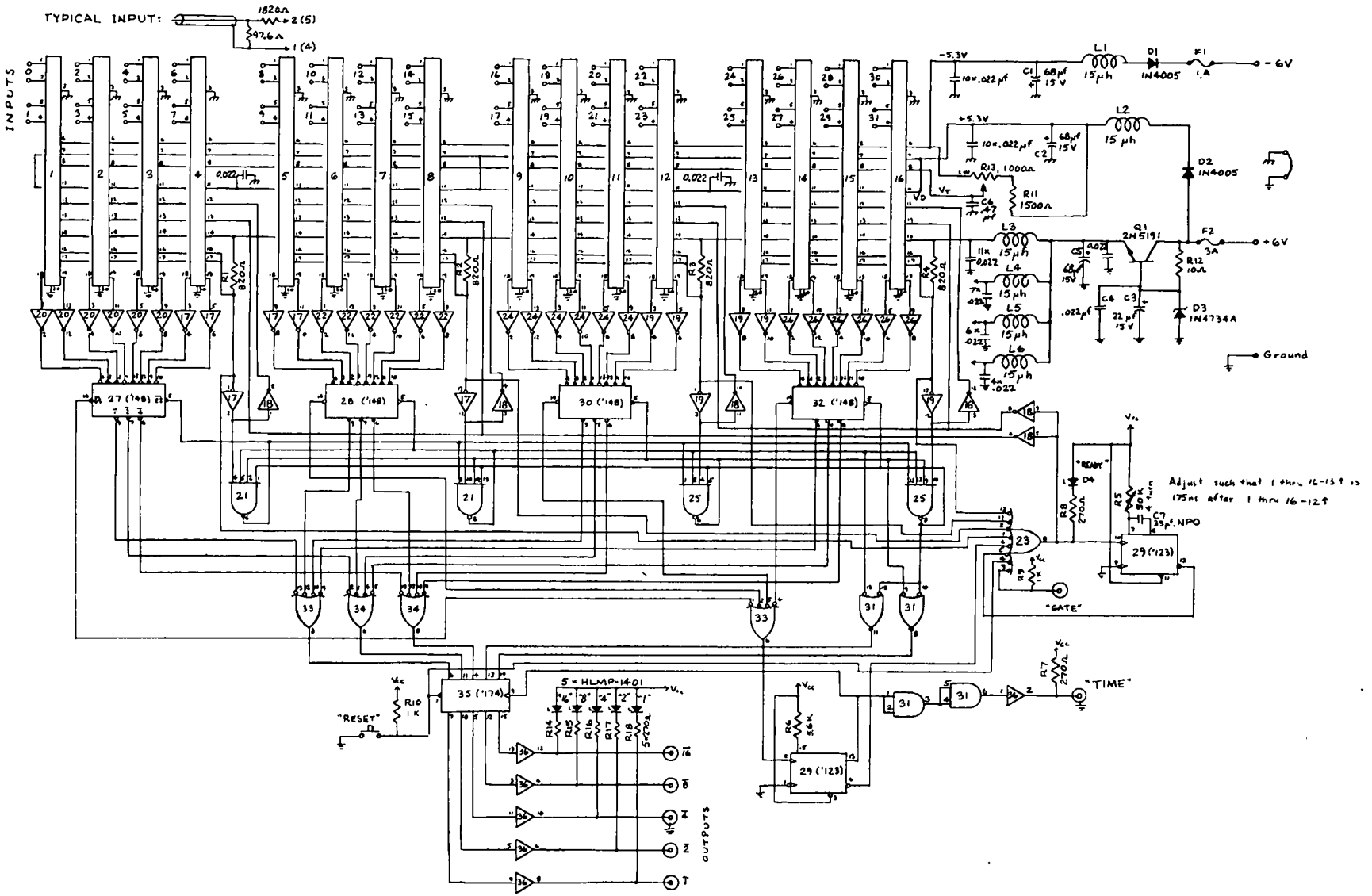


Fig. 5
32-Channel Proportional-Counter Multiplexer (79Y-197902). The circuit is built on a printed-circuit card in a triple-width NIM module.

has a current-sensitive differential input with an impedance of 200 Ω. The discriminator is adjustable over the limited range of 1-5 μA (or 0.2 - 1.0 mV) of the input signal. The delay, intended to allow pretrigger logic in a multiwire detector, is 150 ns (the minimum possible). The latch has both a low-true open-collector output and a high-true TTL level.

An undesirable "feature" of the hybrid circuit is that clearing the latch (low on pin 12) always causes an input pulse; therefore, the gate (pin 13) must be held low after the circuit clears for at least the duration of the 150-ns delay to prevent oscillation. Another annoyance is that although analog and digital power and ground pins are separate, they are interconnected inside the circuit. Of the approximately 6 mA drawn from the delay control (pin 7), 2 mA returns to digital ground and 4 mA to the negative analog power supply (pin 6). About 5.5 mA from the digital V_{CC} (pin 14) also returns through the analog circuit. Because there is a net current of 0.2 mA from the analog ground (pin 3), the analog ground must be returned to power ground on the board.

The multiplexer inputs are four groups of eight signals each. The wire-OR of the open-collector outputs of each group's latches inhibits the other three groups, enables an eight-input priority encoder whose inputs are the latch outputs, turns off all latch gates, and clears the latches in its group. The "Group Select" outputs from the priority encoders generate a pulse to latch the five-bit detector number (low true) and send an output strobe (positive). The low three bits are taken from the priority encoder and the high two bits are the encoded group number.

The duration for which the latches are gated off (the dead time) is set by an on-board potentiometer. It must be long enough to prevent double-pulsing of signals far above threshold, as well as to prevent oscillation; 400 ns should be adequate.

B. Connections

Inputs are through two rear-panel connector blocks; channels 0-15 are on pins 1-16 of the left-hand block (as seen from the front) and channels 16-31 on pins 1-16 of the right-hand block. Use 93-Ω cable (RG-180/U) for each signal, and enclose the bundle in braid connected to the electrostatic shield at the detector end and to the chassis at the multiplexer end. Low-voltage power lines (orange from pin 18, green from pin 19, and violet from pin 20) are twisted together and are run in the same bundle. The high-voltage coaxial cable for detector bias should either be run inside the same braid or tied to it, because the braid is an alternate path for the high-voltage return current (i.e., a ground loop).

Most multiplexers have divide-by-ten attenuators on all inputs, consisting of a 97.6-Ω resistor across the input and an 1820-Ω resistor in series with the internal 200-Ω amplifier input. The front-panel "Threshold" knob then covers the range of 2 mV (knob = 0) to 10 mV (knob = 10). For 1/4-in. detectors, a different attenuator is required: 110 Ω in parallel and 402 Ω in series. The nominal threshold range is then 0.6 mV to 3.0 mV.

Front-panel outputs are the five bits of channel number (low true) and the time strobe (high-true 80-ns pulse). All outputs are open-collector TTL with pull-ups of about 270 Ω. L.E.D.s indicate the number of the last event latched. The "Ready" light is green whenever the unit is "live"; i.e., it is only off during dead time and should appear steady and bright if operation is normal. Grounding the "Gate" input or pushing the "Reset" button disables all signal inputs. The reset button also latches all output bits on (low), thus lighting all the L.E.D.s.

C. Failure Modes

Some information concerning failures is gleaned from output data. A noisy channel may be a bad PC700 chip; count by twos from the rear of the module to find which one. If high-number channels within a block of eight are missing, the 25LS148 is suspect for that group. Another possibility is that the PC700 for the highest number channel containing data may be permanently latched.

A noisy channel may go into oscillation, such that time strobes are issued continuously and the ready light dims. The channel number lights identify the bad channel. Threshold adjustment may be too low, or the dead time too short.

An obscure failure mode is for the ready light to be out (or invisibly dim) but for no time strobes to be generated. We have not duplicated this mode on the bench, and it has never lasted long enough to be diagnosed. Pushing the reset button may speed recovery. The only guaranteed cure is to replace the module.

VI. SECOND-LEVEL MULTIPLEXERS/LINE DRIVERS

The outputs of the 32-channel multiplexer --especially the time-strobe pulses-- will not drive 50-Ω lines, so some form of line driver is required. Three models are available, which have many common features with respect to output and handshaking.

A. Latching Line Driver, 79Y-197953

The circuit is given in Fig. 6. The module is a single-width NIM, and requires 0.9 A at +12 V. It supports a single 32-channel multiplexer.

A pulse on the "Strobe" input latches the five data bits, and after a suitable delay to ensure that the output data lines are set up, an output strobe is generated. Total propagation delay is 80-90 ns; nominal setup time of the outputs before the strobe is 20 ns.

B. Two-Way Multiplexer, 79Y-197955

The circuit is given in Fig. 7. The module is a double-width NIM, and it requires 1.1 A at +12 V; it supports up to 64 detectors.

The channel-number bits and time strobe from one 32-channel multiplexer are connected to the "A" inputs and from another to the "B" inputs. A high-true pulse on either of the "Time" inputs disables the other, selects the corresponding set of five input bits, and starts the time sequence to latch the data (at 30 ns) and to generate an output strobe. If the input was "B", 32 is added to the channel number. Total propagation delay is 90-100 ns; nominal setup time for the outputs before the strobe is at least 15 ns. This module may be used in place of a line driver if the unused time input is grounded.

C. Four-Way Multiplexer, 79Y-197954

The circuit is given in Fig. 8. The module is a triple-width NIM, and requires 1.3 A at +12 V. It supports up to 128 detectors.

Four sets of 32-channel multiplexer outputs are connected to the "A", "B", "C", and "D" inputs, respectively. The five data bits are buffered through noninverting tri-state gates. Each buffer has two additional hard-wired bits to identify the input: "A" = 0, "B" = 32, "C" = 64, and "D" = 96. A strobe on any "Time" input inhibits the other three and enables the

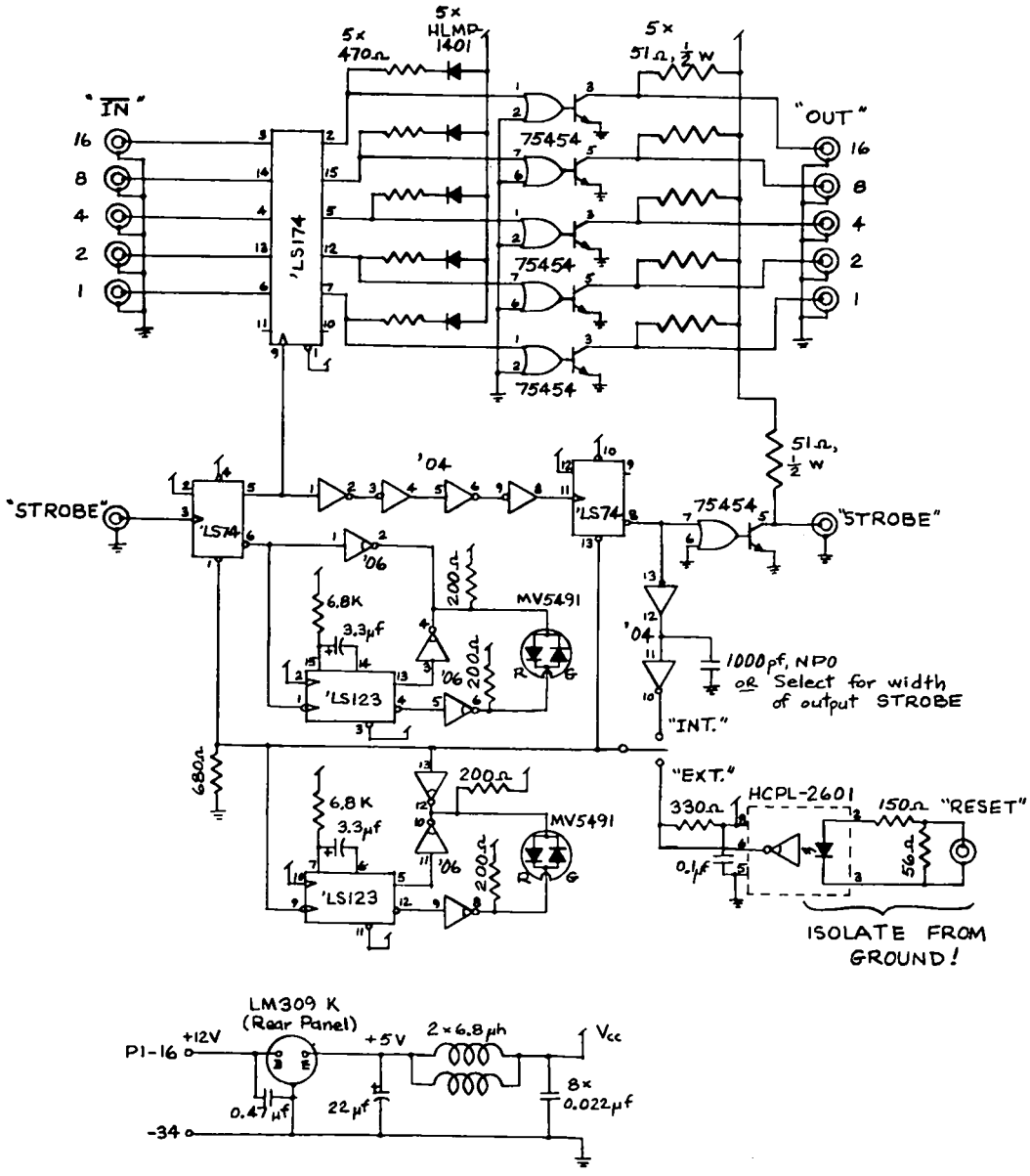


Fig. 6
Latching Line Driver (79Y-197953). The circuit is built in a single-width NIM module using wire-wrap.

corresponding input buffer; if two strobes occur within 3 ns of each other, the circuit may oscillate one or two times before selecting one of the inputs. The logical OR of the four enable signals starts a timing sequence to latch the seven buffered input bits after an appropriate setup time and then to generate an output strobe. Total propagation delay is 100-130 ns and the output data setup time is at least 15 ns before the output strobe. There is a dead time of 180 ns per event. This module may be used in place of a two-way multiplexer or in place of a line driver if unused time inputs are grounded.

D. Outputs and Handshaking

Front-panel yellow L.E.D.s indicate the number of the last detector latched. The output lines are high-true and are maintained at dc levels until

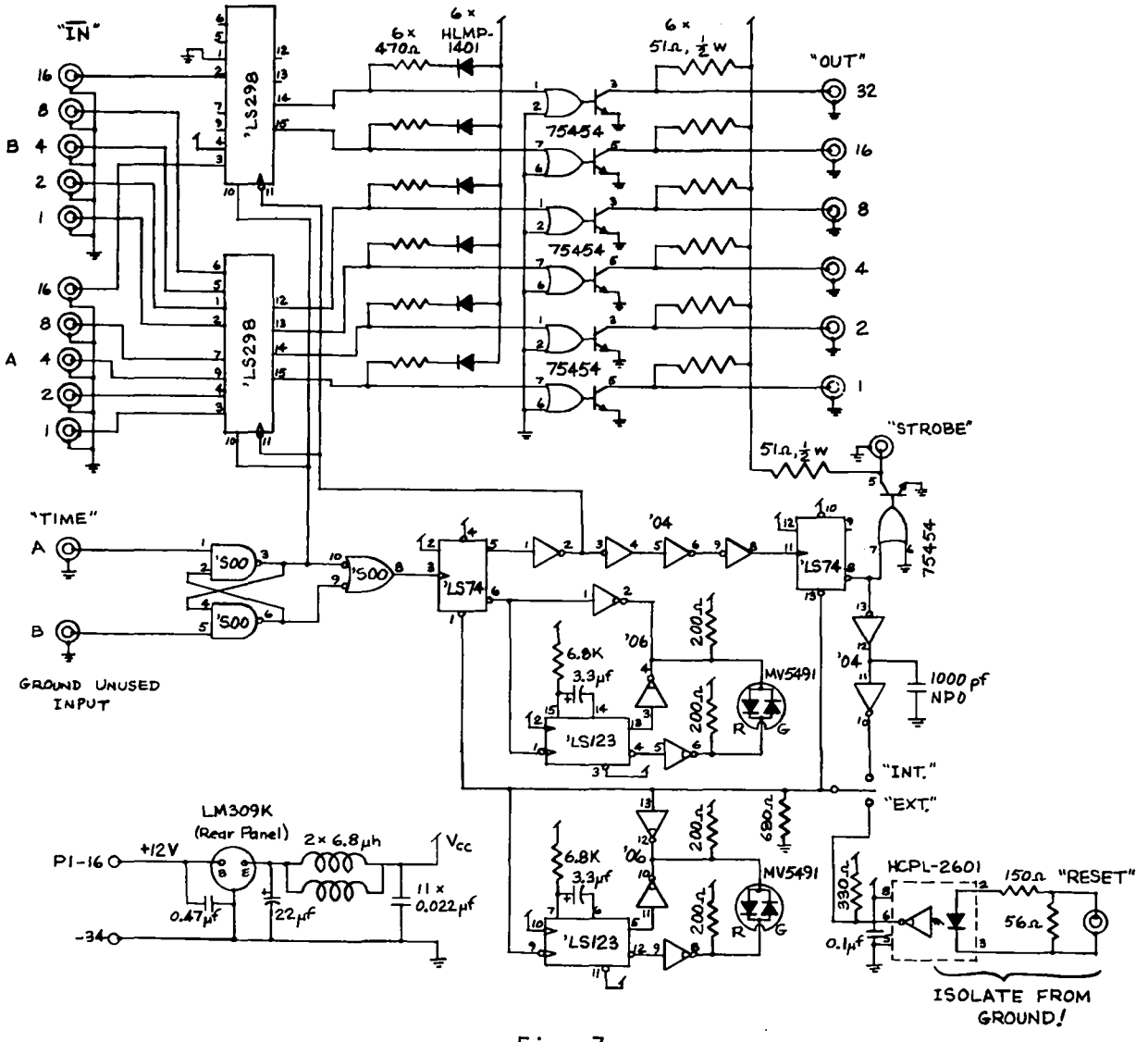


Fig. 7
Two-Way Multiplexer (79Y-197955). The circuit is built in a double-width NIM module using wire-wrap.

the next event is latched. All units use 75454s with 51-Ω pull-up resistors to the +5-V supply to drive all outputs. Thus the high-level output voltage into 50Ω is 2.5 V (current 50 mA). The low-level output is less than 0.4 V if no current is being sunk from the output line, or less than 0.7 V if sinking an additional 200 mA. Outputs will drive 50-Ω cables, such as the RG-217/U used at WNR.

The output "Strobe" signal has an identical driver. It is a high-true pulse whose width may be determined by handshaking. With the front-panel switch set to "INT.", an internal delay is used to reset the output strobe latch and to re-enable the input circuit. In the line driver or two-way multiplexer, the delay is set by choosing a capacitor; in the four-way multiplexer, selection is by wire-wrap to the appropriate tap of the 100-ns TTL delay module. The output pulse must be at least 60 ns wide because of risetime degradation in long cable runs. A nominal 80-ns total width may be required for proper operation of the line receiver module, to ensure adequate

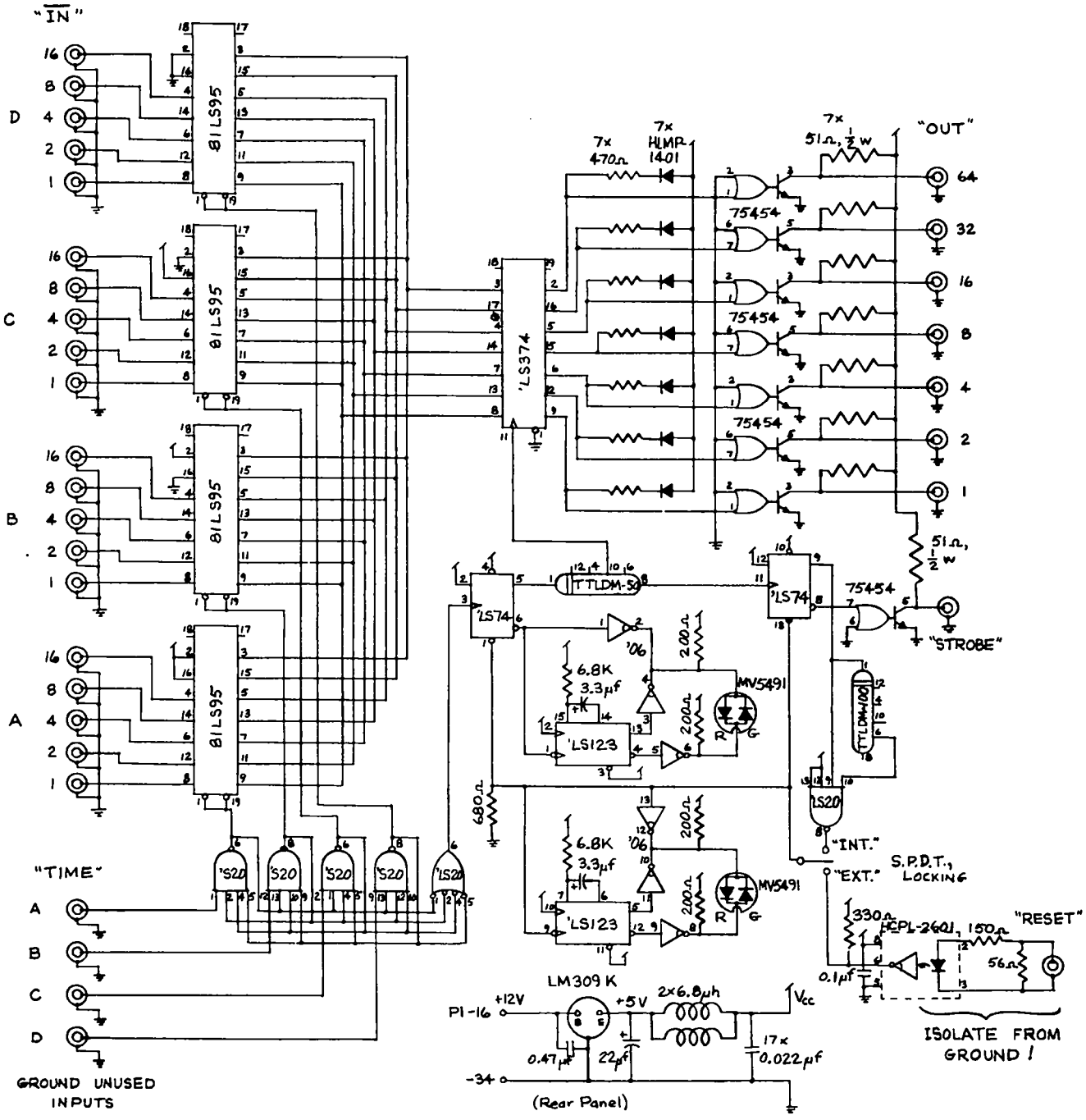


Fig. 8
Four-way Multiplexer (79Y-197954). The circuit is built in a triple-width NIM module using wire-wrap.

deskewing, setup, and hold times for the data lines. Note that the output data lines may start changing about 30 ns after the trailing edge of the strobe output.

With the front-panel switch in the "EXT." position, external handshaking is required. "Strobe" is held high until a high-true (>1.75-V, >33-mA) signal is received on the "Reset" input. This input is isolated optically and is designed to receive a driver circuit similar to this module's outputs. (Hence,

it could be used as a load for testing the output drive capabilities.)

E. Front-Panel Indicators

In addition to the yellow "Data" L.E.D.s, which flicker during normal operation, there are two green/red indicators associated with the "Strobe" and "Reset" signals. Both flash green for about 10 ms for every input pulse and appear green continuously for any reasonable count rate. A red light indicates the presence of a dc level on the line or a failure to reset. (Note for the color-blind 16% of the male population: any light that flickers is almost surely green. A light that remains on with no input is red. Red is brighter than green).

If lights are flickering on the 32-channel multiplexers (indicating that they are sending out pulses) but the two L.E.D.'s are off, ensure that all unused time inputs are grounded (through 50Ω or less). Determine that the module has power and whether the inputs properly connected.

If the strobe L.E.D. is red and the reset L.E.D. is off, the handshake loop is not complete. Switch to "INT."; if the L.E.D. is still red, then look for an internal problem in the latch, delay, or lamp-driver circuits. If not, "EXT." may be tried again. Also try connecting the strobe output directly to the reset input. If the strobe L.E.D. is still (or again) red, suspect the output driver or the optoisolater.

If the reset L.E.D. is ever red or is ever green when the strobe L.E.D. is not green, it indicates spurious levels and/or pulses on the reset signal. If this happens with the switch on "EXT.", trace back along the signal path to determine the cause. Watch for spurious grounds; the braid of this cable should not be grounded locally. If this happens while the switch is on "INT.", something is seriously wrong in the module or in the NIM bin power supplies, and you should expect smoke soon.

VII. ISOLATED LATCH, 79Y-197952

The Isolated Latch is the interface between the cables from the remote multiplexers and the daisy-chain data bus of the Fast Digital Data-Acquisition System (FDDAS). The circuit diagram is given in Fig. 9. The module is built in a double-width CAMAC module, but it has no connection to the CAMAC dataway other than power: 0.6 A at +6 V.

A. Isolation

The first function of the Isolated Latch is to terminate all cables from the experimental area while isolating all signal returns (i.e., isolating all cable braids from local ground). Optical isolators are provided for (up to) eight data lines and for the "Strobe" signal. Data lines are considered true (high) if above 1.7 V (32 mA) and false (low) if less than 1.6 V (30 mA). The strobe input is to be a low-to-high transition, and the threshold is 1.75 V (33 mA). Front-panel test points are provided for the isolated (and inverted) data lines, and the "Delay" output may be monitored as an indicator of the arrival of a strobe pulse. If it is necessary to observe the raw input signals, creation of a ground loop may be avoided by using differential inputs to the oscilloscope.

B. Deskewing

The next function is to correct for skew in the data lines and to initiate the output timing sequence. Because the cable and optoisolator propagation

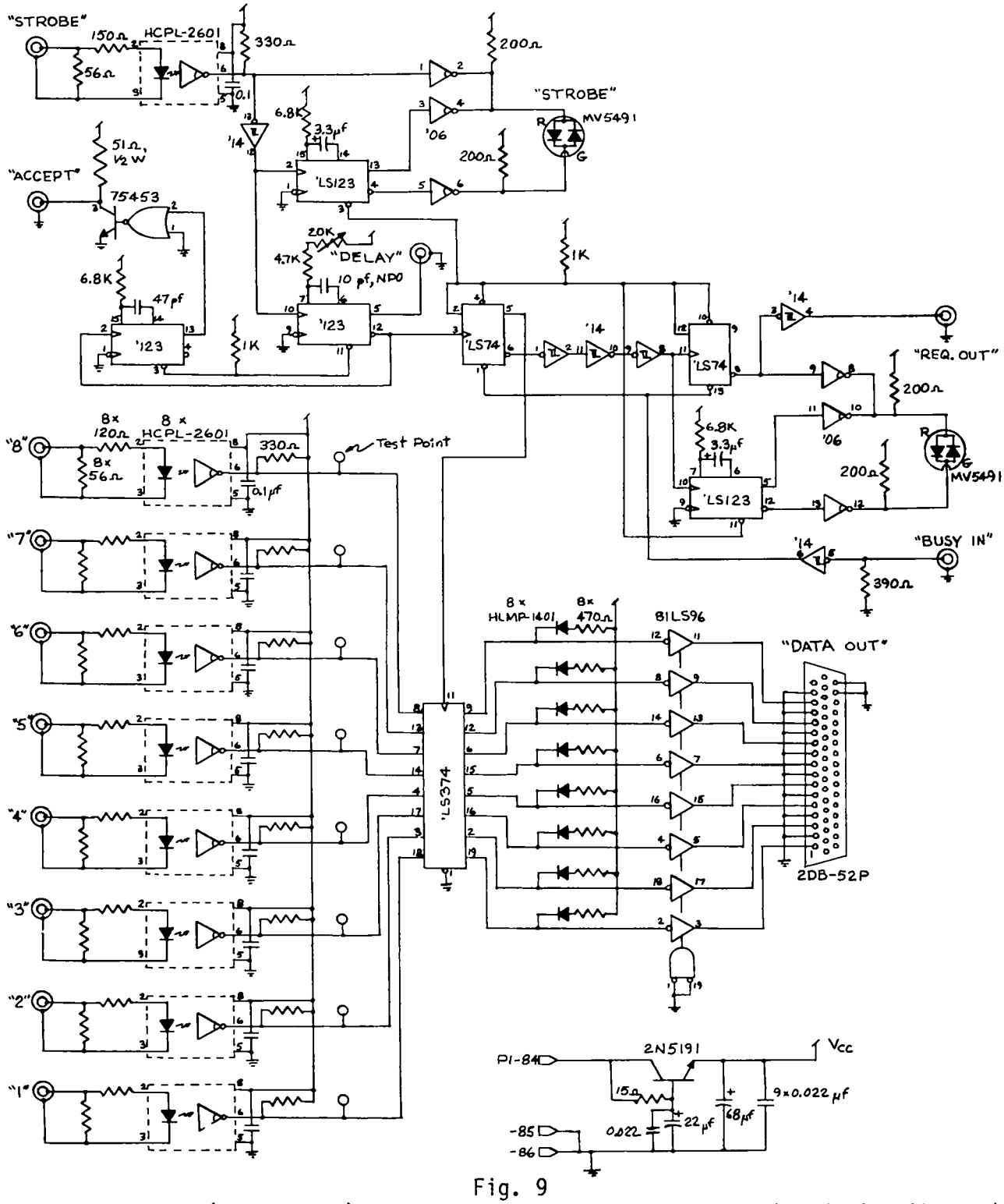


Fig. 9
Isolated Latch (79Y-197952). The circuit is built on a printed-circuit card in a double-width CAMAC module.

times may not be equal for all lines, an adjustable delay is provided to ensure that all data lines are settled before being latched. Adjust the "Delay" potentiometer so that the falling edge of the delay output signal

comes no earlier than 6 ns before all changing data (observed at the test points) are stable at their new values. The data are then latched and should appear at the "Data Out" connector approximately 60 ns after the falling edge of delay. Front-panel yellow L.E.D.s also indicate the contents of the latch. Output data are high-true.

The strobe input pulse must be at least as wide as the delay, to guarantee that the input data will still be valid. See Sec. VI.D.

C. Handshaking and Indicators

At the end of the delay, the circuit generates an "Accept" pulse, which can be sent on 50-Ω cable back to the multiplexer. The pulse is about 100 ns wide and 2.5 V high (50 mA); it may be used as the "Reset" input as described in Sec. VI.D. The "Strobe" L.E.D. flashes green for every strobe input received; if the light is red, the handshaking loop is incomplete. The status of this indicator --off, green, or red-- combined with the two indicators on the line driver (see Sec. VI.E.), gives information on cable continuity. The strobe L.E.D. may be red at power-up or if the strobe input is connected before the accept output; remove and replace the strobe input before looking for other trouble.

Note that the strobe/accept loop is independent of the busy status of the FDDAS handshaking circuit; i.e., the accept pulse will be sent even if the module is hung in the busy state.

The FDDAS consists of a 24-bit unidirectional high-true TTL data bus, two handshaking lines, and some simple timing rules.[1] Data output lines must be set up at least 20 ns before "Request Out" goes high and held for at least 40 ns after "Busy In" is received. The request output must be at least 30 ns wide and may not go high any time that the busy input is high or until 30 ns after the busy input is dropped. The minimum time to transfer one 24-bit data word is 80 ns. A module receiving data should latch the data as soon as it sees a "Request In" and should assert its "Busy Out" for as long as its input latch is occupied. Data is pipelined in the system: each module may start operating on the next event as soon as it has passed the preceding one on. Throughput of the complete system is equal to the slowest module.

In the Isolated Latch, data setup time is provided by three 7414 gates; if more delay is needed, a capacitor may be added at pin 2 (or 11) of the 7414. "Request Out" is latched on by a 74LS74, and held until "Busy In." Note that a busy input prevents any new event from being latched as long as it is high and also holds the request output low. The indicator light will flash green for each request output, will turn red if no busy input is returned, and will be off if the busy input stays high so that no request output can be generated.

VIII. TIME-OF-FLIGHT (T-O-F) CLOCK (MODEL 6), 79Y-197938

Almost all experiments at WNR depend on measuring neutron flight times from source to detector so that the velocities may be determined. For materials science experiments, which use relatively slow neutrons, a rather modest time resolution suffices; however, it is essential to record numerous event timings for each start of the clock, the dead time per event must be low, and the maximum time is a large number of resolution elements. An inexpensive clock was developed to meet these requirements; the current version, which includes both input and output compatible with the FDDAS, is the Model 6 T-O-F Clock. Here are its specifications.

Clock frequency:	20.000 MHz (19.988 MHz in some units)
Start jitter:	50 ns (rms 14 ns)
Dead time:	55–125 ns (mean 90 ns, jitter ±25 ns)
Maximum count time:	1.68 s (2^{24} x 100 ns)
Internal buffer:	16 words x 24 bits
Readout rate:	1 MHz through CAMAC, 8 MHz through FDDAS
Time scales:	Linear, Δt = 100 ns Logarithmic, Δt = Int(1 + t/102.4 μs) x 100 ns Arbitrary, Δt = F(t) by means of custom pROMs

The output of the Clock is a word of 24 bits, selected by internal jumpers from the 24 linear time bits, the 16 nonlinear time bits, and the 24 tag bits from the front-panel "Data In" connector. Figure 10 shows the arrangement of the terminal strips in the Clock. These signals are all high-true; unused high-order bits of the 24-bit descriptor word should be grounded.

Note that the majority of clocks now in use are an earlier version, Model 6A, 79Y-197928[3]. That model has 25 bits on the linear-time jumper strip instead of 24. Use neither the bottom one (100 ns) nor the top four; the smallest channel width is 200 ns and maximum time is 209 ms. There is no prewired logarithmic time scale, and most units do not have the "Data Out" connector wired. The mean dead time in a given clock may be anything between 110 ns and 280 ns, with a jitter of ±50 ns.

A. Strapping for MIDS

To wire the Clock jumpers for a MIDS using a linear time scale, start with the time bit giving the required resolution as the least significant bit of the descriptor word, and continue upward through the 6.55-ms bit (to be able to count for the full 8.33-ms WNR frame). Then use the bottom 8 bits from "Data In," and finally, ground any remaining bits. Users should note the resolution and number of time bits on a tag on the side of the module; these must agree

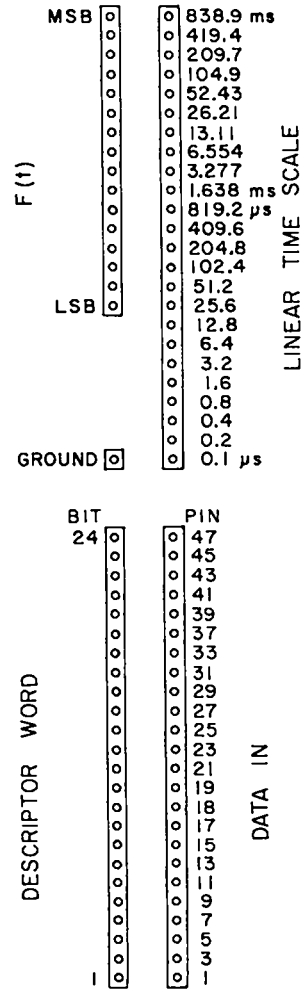


Fig. 10.
Terminal strips in the T-O-F Clock. The 24 bits of the output descriptor word are selected by jumper wires from the linear time scale, the nonlinear time scale F(t), or from the front-panel "Data In" connector. Unused descriptor bits should be grounded.

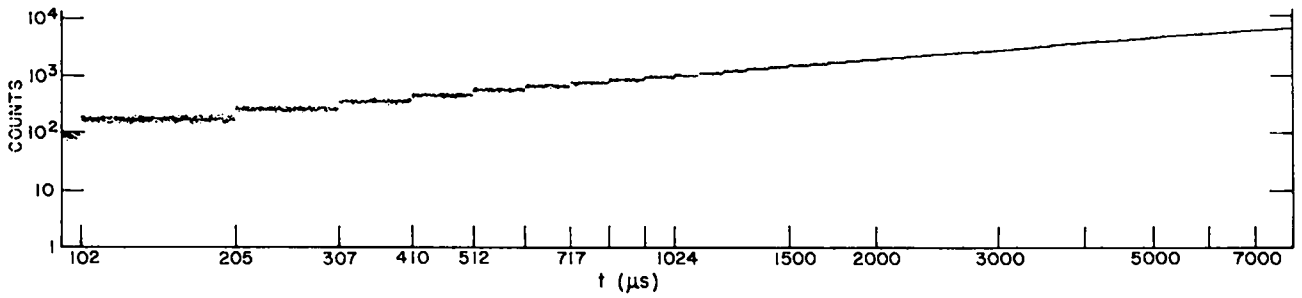


Fig. 11
Logarithmic time scale. A random-time spectrum from a radioactive source is recorded in a 4094-word histogram covering times from 96.0 μs to 7936 μs. Observed counts are proportional to the time-channel width, which starts at 0.1 μs and increases by 0.1 μs every 102.4 μs; the final channels are 7.8 μs wide.

with values provided to the software. The anticipated usual strapping is for a resolution of 1.6 μs, and for 13 time bits, eight tag bits, and three grounds.

To reduce computer memory requirements when many bits are used for detector identification and good time resolution is also required, use the logarithmic time scale. The number of bits needed depends on the "Holdoff" and "Limit" registers. For instance, with holdoff = 96.0 μs and limit = 7936 μs, and 12 bits of F(t) strapped to the descriptor word, a 4094-channel histogram results, with channel width varying from 0.1 μs to 7.8 μs. (See Fig. 11.) A linear time scale with the same number of bits would have a fixed channel width of 3.2 μs (or 1.6 μs if the count duration is less than 6.55 ms); the logarithmic scale maintains a time resolution of 0.1%.

B. Holdoff and Limit Registers

In order to prevent the internal buffer from being filled by γ-ray-induced and very high energy neutron events at T_0, a holdoff is provided following the "Start" input to the Clock before "Request In" inputs will be accepted. The holdoff may be any number from 0 to 255, in units of 6.4 μs (in other words, from 0 to 1632.0 μs). It is written from CAMAC with an A(0)F(16) command. For linear time scales, the Clock begins running at start and the early channels will be empty; for nonlinear scales the first channel does not begin until the end of the holdoff time.

A limit register is used to turn off the Clock and reset it to zero after a fixed time. It is an 8-bit register and may be set to any value from 1 to 255 in units of 51.2 μs (51.2 to 13056.0 μs). It is written from CAMAC with an A(1)F(16) command. Note that if the register contains 0, or a time less than the holdoff, no data can be recorded. Also, note that if count ranges longer than 13 ms are required, the register must be rewired so that the unit is longer than 51.2 μs.

The CAMAC function A(1)F(0) reads both registers; the limit is in the most significant 8 bits and holdoff in the least significant 8 bits of the 24-bit data word. (The middle 8 bits are zero).

C. Front Panel

The bottom half of the panel contains the handshaking and daisy-chain data bus connectors for FDDAS. "Request In", "Busy Out", and "Data In" connect to the Isolated Latch. The L.E.D. next to the request input flashes for any pulse, whether the Clock is running or not. The output-side connections can be used[1] to run a fast histogramming memory (bypassing the CAMAC dataway and the computer I/O bus), for further processing (for example, mapping), or to monitor the data in real time (with digital-to-analog converters and an X-Y monitor scope to display each event). The busy output could be used to monitor the actual dead time. The request output is useful for a watchdog timer, even if the actual Clock output is through CAMAC.

The other essential input to the Clock is "Start", which is a high-true TTL (or 10-V logic) pulse derived from the proton pulse as it reaches the WNR target. The adjacent "On" and "Inhibit" L.E.D.s indicate, respectively, that the Clock is actually running or that start pulses are not being accepted because the CAMAC crate is inhibited.

The "OSC." output allows monitoring of the (free-running) master oscillator in the Clock. It is also possible, by removing the wire jumper at the top of socket D-16, to run a Clock on an external 20-MHz oscillator, such as from another Clock, to guarantee identical channels in several Clocks.

We customarily monitor "Valid", "Lost", and "FIFO Full" in scalers. A 40-ns pulse is produced on the valid output for every event stored in the internal buffer. (Because these may come 50 ns apart, sometimes there may be only a 10-ns gap between pulses and we may lose the second count in the scaler). A count on the lost line indicates that a request input came before the previous one was processed or while the FIFO buffer was full. This should be impossible when the busy output handshaking is connected, but one could run with the Isolated Latch resetting itself to see if any substantial number of counts are being lost. Note that request inputs that come before the Holdoff time or after the limit time are neither valid nor lost.

FIFO Full is a dc level (and a red indicator), which is high (on) whenever the 16-word internal memory is full. Any activity on this line is bad, because we have no way then to correct for dead time. Either reduce the count rate (for example, increase the holdoff) or use a high-speed memory to increase throughput.

D. CAMAC Functions

Any CAMAC cycle addressed to the Clock flashes the "N" light and returns "X". The following are the valid codes.

A(0)F(0)	Read data. Q = 1 if data present; Q = 0 and data = 0 if no data in buffer. LAM turns off when last datum is read.	
A(0)F(16)	Write Holdoff register.	(See Sec. VIII.B.)
A(1)F(16)	Write Limit register.	
A(1)F(0)	Read Holdoff and Limit.	
A(0)F(26)	Enable Clock Start, turn on "Clk. Enable" L.E.D.	
A(0)F(24)	Disable Clock Start, turn off "Clk. Enable" L.E.D.	

A(0)F(27) Test if Clock enabled; Q = 1 if yes, Q = 0 if no.

A(0)F(25) Start Clock (if Enabled), even if the crate is inhibited.

A(0)F(9) Stop Clock, reset to zero.

A(1)F(26) Enable LAM, turn on "LAM Enable" L.E.D.; LAMs will be generated as long as there is any data in the FIFO buffer.

A(1)F(24) Disable LAM, turn off "LAM Enable" L.E.D.; LAM will no longer be generated. No effect on data in buffer.

A(1)F(27) Test if LAM enabled; Q = 1 if yes, Q = 0 if no.

A(1)F(25) Simulate "Request In"; if Clock is running and is between Holdoff and Limit, then store time in FIFO buffer. Turn on "Data" L.E.D.; generate LAM if enabled.

A(1)F(8) Test for LAM; Q = 1 if yes, Q = 0 if no.

A(1)F(11) Clear FIFO; erase any data (thus turning off LAM).

Z Disables Clock Starts, disables LAMs, and clears FIFO.

I Inhibits "Start" pulses; if clock is running, it continues to store data till Limit is reached or till A(0)F(9).

E. Fault Conditions

It is beyond the scope of this report to provide complete trouble-shooting for the T-O-F Clock; however, user input is essential for diagnosis of some problems. The off-line test procedure concentrates on the proper response to CAMAC commands and on logic flow. Problems with the FIFO memory are only apparent in actual operation with "random" data. If trouble is suspected, please note the following.

- Are some channels lower than they should be? Is it every fourth channel every eighth channel, or some recognizable increment?

- How low are they? Are they three-fourths as high as they should be, or are they wrong by some fixed numerical decrement (like 128)?

- Is there an unexpected step (high or low) in the data? At what channel number and time do you find the step?

Plots and/or listings of faulty spectra are very useful.

IX. CONCLUSION

A detailed description of the multiplexers being used at WNR has been given for the benefit of users who wish to know what is in the "black boxes" (white and yellow, in this case) between the experiment and the computer. Features and limitations have been given as a basis for optimization of experimental count rates. Front-panel indicators were described for both monitoring proper operation and localizing faults. External problems such as faulty connections may be solved directly; diagnostic information provided by the user will greatly assist the correction of more complex electronic problems.

ACKNOWLEDGMENTS

I am grateful to Harold Bowen for his assistance in constructing and debugging these modules, and particularly for his great perseverance in solving severe noise problems in the low-level analog sections of the system. I thank John Scheer for his work on the Fast Digital Data-Acquisition System, and for upgrading the T-O-F Clock to Model 6 by adding the FDDAS input and output and the nonlinear time-scale capability. Both men have provided continuous support and suggestions over the development years of the Multiple-Independent Detector System.

REFERENCES

1. R. W. Hendricks, P. A. Seeger, J. W. Scheer, and S. Suehiro, "A Large Capacity, High-Speed Multiparameter Multichannel Analysis System", Nucl. Instrum. Methods 201, 261-279 (1982).

2. Ralph Morrison, Grounding and Shielding Techniques in Instrumentation (John Wiley and Sons, New York, 1967).

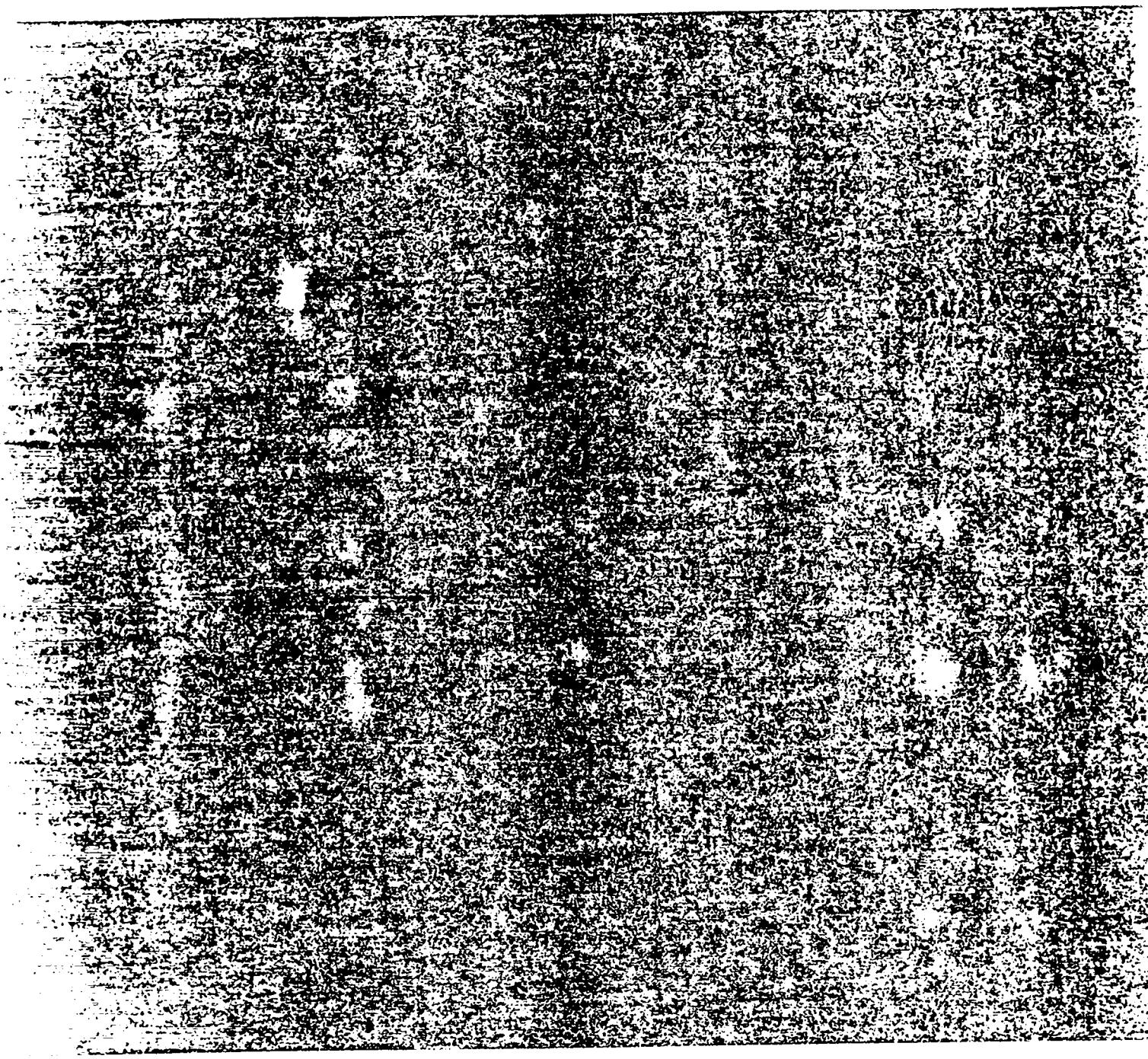
3. J.W. Scheer, "Time of Flight Clock for FDDAS, Model 6", LA-UR-81-1910, presented at the Second National Conference on Synchrotron Radiation Instrumentation, Ithaca, NY, July 15-17, 1981 (unpublished).

Printed in the United States of America
Available from
National Technical Information Service
US Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

Microfiche (A01)

Page Range	NTIS Price Code	Page Range	NTIS Price Code	Page Range	NTIS Price Code	Page Range	NTIS Price Code
001-025	A02	151-175	A08	301-325	A14	451-475	A20
026-050	A03	176-200	A09	326-350	A15	476-500	A21
051-075	A04	201-225	A10	351-375	A16	501-525	A22
076-100	A05	226-250	A11	376-400	A17	526-550	A23
101-125	A06	251-275	A12	401-425	A18	551-575	A24
126-150	A07	276-300	A13	426-450	A19	576-600	A25
						601-up*	A99

*Contact NTIS for a price quote.



Los Alamos